

What is claimed is:

1 1. A test circuit for identification of locations
2 with low speed performance comprising:
3 a grid of units, each unit having a first and second
4 inverter, and the first and second inverter of
5 each unit in a last column being coupled to each
6 other;
7 first switches, each coupled between the first and
8 second inverter of one of the units;
9 second switches, each coupled between the second and
10 first inverter respectively of two adjacent units
11 in a same column;
12 third switches, each coupled between the two first or
13 second inverters of adjacent units in a same row;
14 pairs of serially connected fourth switch and third
15 inverter, each coupled between the first and
16 second inverter of one of the units in a first
17 column; and
18 pairs of serially connected fifth switch and fourth
19 inverter, each coupled between the second and
20 first inverter respectively of a last and first
21 unit in a same column.

1 2. The test circuit as claimed in claim 1, wherein
2 the locations with low speed performance are identified
3 according to frequencies of oscillation signals generated by
4 rows of ring oscillators formed by opening the first, second
5 and fifth switches, and closing the third and fourth
6 switches, and columns of ring oscillators formed by closing

7 the first, second and fifth switches, and opening the third
8 and fourth switches.

1 3. The test circuit as claimed in claim 1, wherein
2 the first and second inverters are inverter strings having
3 the same number of inverters.

1 4. The test circuit as claimed in claim 1, wherein
2 the first and second inverter of one of the units are
3 inverter strings comprising an even number of inverters.

1 5. A test circuit for identification of locations
2 with low speed performance comprising:
3 a grid of units, each unit having a first and second
4 inverter, and the first and second inverter of
5 each unit in a last column being coupled to each
6 other;
7 first transistors, each having a drain and source
8 respectively coupled to the first inverter and
9 the second inverter of one of the units;
10 second transistors, each having a drain and source
11 respectively coupled to the second and first
12 inverter of two adjacent units in a same column;
13 third transistors, each having a drain and source
14 respectively coupled to the two first or second
15 inverters of adjacent units in a same row;
16 pairs of serially connected fourth transistor and third
17 inverter, each coupled between the first and
18 second inverter of one of the units in a first
19 column; and

20 pairs of serially connected fifth transistor and fourth
21 inverter, each coupled between the second and
22 first inverter of a last and first unit in a same
23 column; and
24 a switch control circuit generating gate signals to
25 gates of all the transistors.

1 6 The test circuit as claimed in claim 5, wherein
2 the locations with low speed performance are identified
3 according to frequencies of oscillation signals generated by
4 rows of ring oscillators formed by the switch control
5 circuit turning off the first, second and fifth transistors,
6 and turning on the third and fourth transistors, and columns
7 of ring oscillators formed by the switch control circuit
8 turning on the first, second and fifth transistors, and
9 turning off the third and fourth transistors.

1 7. The test circuit as claimed in claim 5, wherein
2 the first and second inverters are inverter strings having
3 the same number of inverters.

1 8. The test circuit as claimed in claim 5, wherein
2 the first and second inverters of one of the units are
3 inverter strings having an even number of inverters.

1 9. The test circuit as claimed in claim 5, wherein
2 the gates of the third transistors are coupled to receive a
3 control signal and the switch control circuit comprises:

4 a string of fifth inverters receiving the control
5 signal, each of which has an input and output

6 terminal respectively coupled to the gates of the
7 adjacent fourth and second transistors;
8 a sixth inverter has an input and output terminal
9 respectively coupled to the gates of the adjacent
10 fourth and fifth transistors; and
11 a seventh inverter has an output terminal coupled to
12 all the gates of the first and second
13 transistors, and an input terminal coupled to
14 receive the control signal.

1 10. A test circuit for identification of defect
2 locations resulting in low speed performance comprising:
3 a grid ring oscillator capable of detecting a
4 propagation delay through vertical and horizontal
5 branch circuits; and
6 circuitry for evaluating test results of both the
7 vertical and horizontal branch circuits to
8 identify critical locations with low speed
9 performance.

1 11 The test circuit as claimed in claim 10, wherein
2 the grid ring oscillator comprises:
3 a grid of units, each unit having a first and second
4 inverter, and the first and second inverter of
5 each unit in a last column being coupled to each
6 other;
7 first switches, each coupled between the first and
8 second inverter of one of the units;

9 second switches, each coupled between the second and
10 first inverter respectively of two adjacent units
11 in a same column;
12 third switches, each coupled between the two first or
13 second inverters of adjacent units in a same row;
14 pairs of serially connected fourth switch and third
15 inverter, each coupled between the first and
16 second inverter of one of the units in a first
17 column; and
18 pairs of serially connected fifth switch and fourth
19 inverter, each coupled between the second and
20 first inverter respectively of a last and first
21 unit in a same column.

1 12. The test circuit as claimed in claim 11, wherein
2 the locations with low speed performance are identified
3 according to frequencies of oscillation signals generated by
4 rows of ring oscillators formed by opening the first, second
5 and fifth switches, and closing the third and fourth
6 switches, and columns of ring oscillators formed by closing
7 the first, second and fifth switches, and opening the third
8 and fourth switches.

1 13. The test circuit as claimed in claim 11, wherein
2 the first and second inverters are inverter strings having
3 the same number of inverters.

1 14. The test circuit as claimed in claim 11, wherein
2 the first and second inverter of one of the units are
3 inverter strings comprising an even number of inverters.

1 15. The test circuit as claimed in claim 10, wherein
2 the grid ring oscillator comprises:
3 a grid of units, each unit having a first and second
4 inverter, and the first and second inverter of
5 each unit in a last column being coupled to each
6 other;
7 first transistors, each having a drain and source
8 respectively coupled to the first inverter and
9 the second inverter of one of the units;
10 second transistors, each having a drain and source
11 respectively coupled to the second and first
12 inverter of two adjacent units in a same column;
13 third transistors, each having a drain and source
14 respectively coupled to the two first or second
15 inverters of adjacent units in a same row;
16 pairs of serially connected fourth transistor and third
17 inverter, each coupled between the first and
18 second inverter of one of the units in a first
19 column; and
20 pairs of serially connected fifth transistor and fourth
21 inverter, each coupled between the second and
22 first inverter of a last and first unit in a same
23 column; and
24 a switch control circuit generating gate signals to
25 gates of all the transistors.

1 16 The test circuit as claimed in claim 15, wherein
2 the locations with low speed performance are identified
3 according to frequencies of oscillation signals generated by

4 rows of ring oscillators formed by the switch control
5 circuit turning off the first, second and fifth transistors,
6 and turning on the third and fourth transistors, and columns
7 of ring oscillators formed by the switch control circuit
8 turning on the first, second and fifth transistors, and
9 turning off the third and fourth transistors.

1 17. The test circuit as claimed in claim 15, wherein
2 the first and second inverters are inverter strings having
3 the same number of inverters.

1 18. The test circuit as claimed in claim 15, wherein
2 the first and second inverters of one of the units are
3 inverter strings having an even number of inverters.

1 19. The test circuit as claimed in claim 15, wherein
2 the gates of the third transistors are coupled to receive a
3 control signal and the switch control circuit comprises:
4 a string of fifth inverters receiving the control
5 signal, each of which has an input and output
6 terminal respectively coupled to the gates of the
7 adjacent fourth and second transistors;
8 a sixth inverter has an input and output terminal
9 respectively coupled to the gates of the adjacent
10 fourth and fifth transistors; and
11 a seventh inverter has an output terminal coupled to
12 all the gates of the first and second
13 transistors, and an input terminal coupled to
14 receive the control signal.